(FILE 'HOME' ENTERED AT 16:12:22 ON 13 FEB 2004)

FILE 'REGISTRY' ENTERED AT 16:14:00 ON 13 FEB 2004

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L1         19828 S O.SI/MF OR O SI/ELF
L2            48 S O2 SI/MF
L3           368 S N.O.SI/MF OR N O SI/ELF
L4           812 S N.SI/MF OR N SI/ELF
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FILE 'HCAPLUS' ENTERED AT 16:19:13 ON 13 FEB 2004

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L5        450447 S L1 OR (SILICON()OXIDE OR SI03)
L6        674560 S L2 OR (SILICON()DIOXIDE OR SIO2 OR SILICA)
L7          4949 S L3 OR SILICON()OXYNITRIDE
L8         68469 S L4 OR (NITRID? OR NITROGEN?)()SILICA
L9        799173 S L5-L8
L10         3190 S L9 AND PASSIVAT? (3N)(LAYER? OR FILM? OR COAT? OR MULTILAYER?
L11           14 S L10 AND PASSIVAT?(3N)(HARD? OR SOFT?)
L12         3176 S L10 NOT L11
L13          222 S L12 AND POLYIMIDE
L14            1 S L13 AND (PHOTODEFIN? OR PHOTO()DEFIN?)(3N)POLYIMIDE
L15          221 S L13 NOT L14
L16           80 S L15 AND (INSULAT? OR DIELECTR?)(3N)(LAYER? OR FILM? OR COAT?
L17           18 S L16 AND (ADHESI? OR ADHERE? OR STICK? OR CLING? OR BOND? OR C
L18           62 S L16 NOT L17
L19            3 S L18 AND (PLASMA()ENHANC?()CHEMICAL()VAPOR()DEPOSITION OR PECV
```

L11 ANSWER 1 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:106074 HCAPLUS
DN 138:307388
TI Constitutive response of **passivated** copper **films** to thermal cycling
AU Shen, Y.-L.; Ramamurty, U.
CS Department of Mechanical Engineering, University of New Mexico, Albuquerque, NM, 87131, USA
SO Journal of Applied Physics (2003), 93(3), 1806-1812
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB The thermomech. behavior of **passivated** thin copper **films** is studied. Stresses in copper films of thickness ranging from 125 to 1000 nm, deposited on quartz or silicon substrates and passivated with **silicon oxide**, were measured using the curvature method. The thermal cycling spans a temperature range from -196 to 600°C. The measured mech. behavior was found to be rate insensitive within the heating/cooling rate range of 5-25°C/min. It was observed that the **passivated films** do not exhibit a significant stress relaxation at elevated temps. that is normally found in unpassivated films. Furthermore, a significant strain hardening during the course of thermal loading was noted. Simple continuum plasticity analyses show that the exptl. measured stress-temperature response can only be rationalized with a kinematic hardening model. Anal. procedures for extracting the constitutive properties of the films that were developed on the basis of such a model are presented. The initial yield strength is higher and tends to be less temperature dependent in thinner films. The strain hardening rate is found to increase with decreasing film thickness.
RE.CNT 37 THERE ARE 37 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 2 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:556075 HCAPLUS
DN 137:118026
TI Method of forming a bit line and a node contact hole
IN Chern, Horng-Nan; Lin, Kun-Chi
PA Taiwan
SO U.S. Pat. Appl. Publ., 8 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002098699	A1	20020725	US 2001-764335	20010119
US 2001-764335		20010119		

PI
PRAI
AB The invention relates to a process for making a DRAM integrated circuit. A first and a second dielec. layer are first formed on a substrate of a semiconductor wafer. A landing pad is then formed in the first dielec. layer, and a plurality of openings used in the formation of the bit lines are formed penetrating from the second dielec. layer through to the surface of the first dielec. layer. A conductive layer is then formed to cover the surface of the semiconductor wafer and filling in the openings in the second dielec. layer. An etching back process is then performed to remove portions of the conductive layer so the surface of the conductive

layer is lower than that of the second dielec. layer, and the resulting residual conductive layer within the openings form the bit lines. An etching process is performed to form a passivation recess in the second dielec. layer atop each bit line, followed by the formation of a **passivation layer** in the **passivation** recess.
A third dielec. layer is then formed on the second dielec. **layer** and covering the **passivation layers** on the bit lines.
Finally, using the **passivation layers** as **hard** masks, the node contact hole is formed within both the second and the third dielec. layer.

L11 ANSWER 3 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:505331 HCAPLUS
DN 137:71429
TI Method and structure to reduce the damage associated with programming electrical fuses in FPGA IC
IN Kothandaraman, Chandrasekharan; Stetter, Michael; Iyer, Sundar K.
PA USA
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002086462	A1	20020704	US 2000-751475	20001228
	US 6432760	B2	20020813		
PRAI	US 2000-751475		20001228		

AB An improved fuse structure in an integrated circuit (IC) structure is made by forming a gate stack comprised of layers of polysilicon and a silicide. Subsequent to the formation of the silicide layer, an etch stop silicon nitride layer is deposited over the silicide layer. The silicon nitride layer is patterned to expose the silicide layer. A **soft passivation layer** is deposited over the exposed silicide layer. The **soft passivation layer** has a low thermal conductivity which confines energy in the silicide layer, minimizing the current needed to program the fuse. The inherent ductility of the **soft passivation layer** prevents the generation of cracks in the surrounding layers.

L11 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:256922 HCAPLUS
DN 136:376307
TI Effect of pH on chemical-mechanical polishing of copper and tantalum
AU Jindal, Anurag; Li, Ying; Babu, S. V.
CS Departments of Chemical Engineering, Center For Advanced Materials Processing, Clarkson University, Potsdam, NY, 13699, USA
SO Materials Research Society Symposium Proceedings (2001), 671(Chemical-Mechanical Polishing 2001--Advances and Future Challenges), M6.8/1-M6.8/6
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB PH has a strong effect on the polish rates of Cu and Ta. In this paper, removal rates of Cu and Ta using aqueous slurries containing alumina and **silica** abrasives in H2O2-glycine solution are studied at varying pH

values. Variation in the Cu and Ta removal rates is a direct result of the change in surface characteristics of the films. Surface characteristics such as presence/absence of a **passivating layer** and **hardness** of such layer vary with pH and hence result in removal rate variation. A favorable Cu/Ta polish rate selectivity can be obtained by adjusting the pH of the slurry.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:163838 HCAPLUS
DN 136:209188
TI Passivation deposition process for improving interfacial adhesion between oxide and **hard passivation layers** to prevent delamination in integrated circuits
IN Seshan, Krishna; Dass, M. Lawrence A.; Bakker, Geoffrey L.
PA Intel Corporation, USA
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6352940	B1	20020305	US 1998-105590	19980626
PRAI US 1998-105590		19980626		

AB A method of passivating an integrated circuit (IC) is provided. An insulating layer is formed onto the IC. An adhesion layer is formed onto a surface of the insulating layer by treating the surface of the insulating layer with a gas and gas plasma. A 1st **passivation layer** is formed upon the adhesion **layer**, the 1st **passivation layer** and the gas and gas plasma including at least one common chemical element.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:771134 HCAPLUS
DN 135:296660
TI Finite-element analysis of stress effect in metallization/ **passivation layers** during thermal cycling
AU Lee, So-Yoon; Jeong, Jeung-Hyun; Kwon, Dongil
CS School of Materials Science and Engineering, Seoul National University, Seoul, 151-742, S. Korea
SO Taehan Kumsok, Chaeryo Hakhoechi (2001), 39(8), 949-955
CODEN: TKHABB
PB Korean Institute of Metals and Materials
DT Journal
LA Korean
AB Electronic pads and interconnects consisting of a **passivation layer** (**hard layer**) and a metal layer (ductile layer), e.g. SiN/Al/**SiO2**/Si, are very important m many electronic devices. However, they are likely to fail due to cracking of the **passivation layers** during operation of the devices. This study investigates the failure mechanism through finite-element anal. (FEA). FEA calcns. reveal that residual stress is produced in the **passivation layer** as a result of thermal cycling and increases as cycling continues. During thermal

cycling, the multilayer films are deformed by various stresses due to differential thermal expansion of adjacent materials, particularly shear stresses applied to the chip (or die) surface by the large thermal mismatch between substrate and chip (or die). The cyclic shear stress leads to accumulation of asym. plastic deformation (called the ratcheting effect) in the metal layers. The residual strain or stress in the **passivation layer** may be induced by the ratcheting deformation of metal layer. The effects of the thickness and the yield stress of the **passivation** and metal **layers** were analyzed through FEA and discussed. The residual stress in the **passivation layer** decreases with **passivation layer** thickness and metal layer yield strength, which is closely related to the likelihood of plastic yielding in the metal layer.

L11 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:694002 HCAPLUS
DN 129:338171
TI The effect of overlayers on the stability of discontinuous silver films deposited on softened poly(2-vinylpyridine) substrates
AU Pattabi, Manjunatha; Mohan Rao, K.
CS Materials Science Department, Mangalore University, Mangalagangotri, 574 199, India
SO Journal of Physics D: Applied Physics (1998), 31(19), 2412-2415
CODEN: JPAPBE; ISSN: 0022-3727
PB Institute of Physics Publishing
DT Journal
LA English
AB Results of studies on the effect of inorg. overlayers on the long-term stability of discontinuous Ag films deposited on softened poly(2-vinylpyridine) (PVP) substrates are reported. Discontinuous Ag films were evaporated onto PVP-coated glass substrates held at 425 K in a vacuum of 8 + 10-6 torr. The films were coated with overlayers of Al2O3, **SiO2** and ZrO2 prior to exposure to the atmospheric The stability of the films against exposure to the atmospheric was studied by monitoring the resistance during and after exposure to the atmospheric The stability was monitored for a period of 120 days and the film's resistance had stabilized by 30 days. Overlayers improve the stability considerably and **SiO2** seems to be the best passivator, closely followed by ZrO2. However, compared to Al2O3, ZrO2 gives better protection even with a smaller overlayer thickness. A stable discontinuous film with a gauge factor of .apprx.30 could be prepared by depositing Ag onto **softened** PVP **passivated** by an overlayer, after 30 days of ageing.
RE.CNT 28 THERE ARE 28 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 8 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:772997 HCAPLUS
DN 123:185626
TI Passivation method and structure for a ferroelectric integrated circuit using hard ceramic materials or the like
IN Argos, George, Jr.; Spano, John D.; Traynor, Steven D.
PA Ramtron International Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

PI	US 5438023	A	19950801	US 1994-212495	19940311
	US 5578867	A	19961126	US 1995-394467	19950227
	JP 08055850	A2	19960227	JP 1995-52145	19950313
	JP 2921556	B2	19990719		
PRAI	US 1994-212495		19940311		

AB A method for passivating an integrated circuit includes the RF sputtering of a **hard passivation layer** on the surface of the integrated circuit. The **hard passivation layer** can be a ceramic material such as various doped and undoped titanates, zirconates, niobates, tantalates, stannates, hafnates, and manganates, in either their ferroelec. or nonferroelec. phases. Other exotic, hard, and usually nonferroelec. materials not normally found in integrated circuit processing, such as carbides, may also be used. If the integrated circuit sought to be passivated contains ferroelec. devices, the **hard passivation layer** can be fabricated out of the same material used in the integrated ferroelec. devices. An optional **SiO2** insulating layer can be deposited on the surface of the integrated circuit before the **hard passivation layer** is deposited. The optional **SiO2** layer is used to prevent any possible contamination of the integrated circuit by the **passivation layer**. Similarly, an optional sealing layer such as **SiO2**, Si nitride, or polymer-based materials can be deposited on top of the **passivation layer** to prevent any possible contamination of the integrated circuit package by the **passivation layer**. Once the **hard passivation layer** and any optional layers are formed, these layers are etched to provide access to underlying integrated circuit bonding pads.

L11 ANSWER 9 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:401540 HCAPLUS
DN 122:327607
TI A radiation-hardened 32-bit microprocessor based on the commercial CMOS process
AU Yoshioka, Shinichi; Kamimura, Hiroshi; Akiyama, Masatsugu; Nakamura, Mitsuhiro; Tamura, Takashi; Kuboyama, Satoshi
CS Hitachi, Ltd., Tokyo, 101-10, Japan
SO IEEE Transactions on Nuclear Science (1994), 41(6, Pt. 1), 2481-6
CODEN: IETNAE; ISSN: 0018-9499
DT Journal
LA English
AB A radiation-hardened 32-bit microprocessor based on the com. CMOS process, usable up to 1 kGy(Si), was developed by (1) adding a Si nitride **passivation layer** and (2) thinning the field oxide. Both techniques suppress the leakage current generated by the parasitic MOSFET, because its neg. threshold voltage shift due to oxide trapped holes is decreased by the letter, and compensated by the pos. shift due to the interface states generated during irradiation by H trapped in the oxide through the Si-nitride deposition. The samples supplied with 4.5 V and 20 MHz clock were able to operate normally up to the total dose of 1.3 kGy(Si). The total dose tolerance of the samples was over 20 times as much as that of ones based on the com. process.

L11 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1992:133661 HCAPLUS
DN 116:133661
TI Electrochemical aspects of erosion-corrosion in particle-containing

liquids
AU Ehmann, I.; Heitz, E.; Schnitzler, A.
CS Dechema-Inst., Frankfurt/Main, W-6000/97, Germany
SO Werkstoffe und Korrosion (1991), 42(10), 520-7
CODEN: WSKRAT; ISSN: 0043-2822
DT Journal
LA German
AB The erosion corrosion of 8 steels in flowing particle-containing liqs. (gypsum and quartz particles, chloride medium, pH 2-7) from flue gas desulfurization was studied by measurement of electrochem. polarization curves. The reciprocal polarization resistance was proportionalto the material loss. The abrasive material loss was determined by the **hardness** of the **passivation layer** and not by the hardness of the base materials.

L11 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1991:645596 HCAPLUS
DN 115:245596
TI Aluminum diffusion into glass **films** used for the **passivation** of fine Al metalization
AU Tanikawa, A.
CS Microelectron. Res. Lab., NEC Corp., Kanagawa, 216, Japan
SO Journal of the Electrochemical Society (1991), 138(10), 3047-9
CODEN: JESOAN; ISSN: 0013-4651
DT Journal
LA English
AB Energy-dispersive x-ray spectroscopy anal., performed using anal. electron microscopy, was conducted on **films** used for the **passivation** of fine Al metalizations in order to determine the source of stress-induced voiding. The anal. detected Al in the **passivation films** at levels approx. 2-3% of the original total Al metalizations, which suggests diffusion of Al into the **passivation film** as a possible source of the stress which induces voiding, and/or as a possible origin of change in volume and **hardness** of the **passivation film**.

L11 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1988:140434 HCAPLUS
DN 108:140434
TI Passivated optical fibers for harsh environments
AU Skutnik, B. J.; Hodge, M. H.; Clarkin, J. P.
CS Ensign-Bickford Opt. Co., Avon, CT, 06001, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1988), 842(Fiber Opt. Reliab.: Benign Adverse Environ.), 162-8
CODEN: PSISDG; ISSN: 0277-786X
DT Journal
LA English
AB Glass optical fibers have high strengths but under tensile stress and in the presence of aqueous media their strength diminishes through fatigue. Analogous to the semiconductor field, where the electronic properties of chips are protected by **passivating coatings**, optical fiber strength can be protected by passivating the glass surface. Optical fibers have been developed with such a primary coating/cladding, namely hard clad **SiO2** fibers. These fibers have high initial strength and good fatigue resistance. Their stability to environmental exposure is demonstrated by comparing static fatigue results for exposure to hot and boiling H2O, to steam and to acid/base solns. ranging from 10 M acid to 10 M base to results obtained in ambient H2O. Hard clad **SiO2**

fibers maintain high static fatigue parameters at elevated temps. and exposure to these temps. under low stress does not change their fatigue behavior. Except at the extremes in pH, the static fatigue behavior is unchanged across the acid/base spectrum. This insensitivity to environmental changes and the good fit of the data to the power law model permits the prediction of lifetimes for long term exposure to aqueous environments.

L11 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1983:153669 HCAPLUS
DN 98:153669
TI Semiconductor device
PA Nippon Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 57199224	A2	19821207	JP 1981-84758	19810602
	JP 63056704	B4	19881109		
PRAI	JP 1981-84758		19810602		

AB During the fabrication of a semiconductor device with a Si3N4 **passivation layer**, an addnl. insulator layer from a material (e.g., a low-m.p. glass) with a softening point lower than the m.ps. of the materials comprising the device is provided under the Si3N4 layer to prevent the Si3N4 layer from cracking.

L11 ANSWER 14 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1981:416518 HCAPLUS
DN 95:16518
TI Effects of conductor passivation on bubble propagation in contiguous disk devices
AU Horng, C. T.; Schwenker, R. O.
CS IBM Res. Lab., San Jose, CA, 95193, USA
SO Journal of Applied Physics (1981), 52(3, Pt. 2), 2383-5
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB The impact was investigated of conductor passivation on 1-μm bubble propagation in contiguous disk devices. Without conductor passivation, devices with overlying AlCu stripes show good propagation margins. When the devices are **passivated** with a thick **layer** of **SiO2**, the elastically "hard" dielec. material imposes a constraint to AlCu deformation and increases the conductor edge force. Furthermore, the edge force of the **SiO2** passivation at the conductor edges, being in the same sign as that of the AlCu stripe, contributes to the total force acting on the underlying garnet. This intensifies the local stress fields in the magnetic devices and seriously reduces the bubble propagation margin. To alleviate this passivation-enhanced stress problem, contiguous disk devices were **passivated** by elastically "**soft**" polyimide instead of sputtered **SiO2**.

L14 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:204050 HCAPLUS
DN 136:387440
TI A new aqueous developable positive tone **photodefinable polyimide** for a stress buffer coat of semiconductor; HD-8000
AU Nunomura, Masataka; Ohe, Masayuki
CS Yamazaki Research & Development Center, Hitachi Chemical DuPont Micro Systems Co. Ltd., Hitachi, 317-8555, Japan
SO Journal of Photopolymer Science and Technology (2001), 14(5), 717-722
CODEN: JSTEEW; ISSN: 0914-9244
PB Technical Association of Photopolymers, Japan
DT Journal
LA English
AB A new aqueous developable pos. tone **photodefinable polyimide** was prepared from poly(hydroxy amic acid) and naphthoquinonediazide for semiconductor stress buffer coat, which exhibits excellent photolithog. properties in high resolution, wide focus latitude and good stability for process holding time, with equivalent film properties to conventional non-**photodefinable polyimide**. Through dry etching evaluation of the SiN **passivation layer**, it was confirmed that the cured **polyimide** pattern works as an etching mask.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 1 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:784647 HCAPLUS
DN 139:284828
TI Design of an electronic package having a light shield for protecting photosensitive surface mount devices
IN Ignaut, Sharon L.
PA National Semiconductor Corporation, USA
SO U.S., 20 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6630736	B1	20031007	US 2000-627043	20000727
PRAI US 2000-627043		20000727		

AB The invention relates to the design of an electronic package having a light shield for protecting photosensitive surface mount devices, where the devices are not fully encapsulated or are encapsulated in a resilient transparent coating. The integrated circuit package includes at least a substrate and a light shield. The substrate has an integrated circuit formed on its surface. The integrated circuit includes light sensitive areas, which are adversely affected by ambient light. The light shield is disposed over the light sensitive portions to block ambient light from reaching the light sensitive portions of the circuit so that the elec. characteristics of the circuit are not significantly altered when the circuit is operated in ambient light. The integrated circuit package also includes a plurality of **bond** pads disposed on the substrate surface and a first **passivation layer** disposed between the **bond** pads and the light shield and between the substrate surface and the light shield. The light shield is arranged to extend over the edge of the **bonding** pad. Further still, the integrated circuit package includes a second **passivation layer** disposed over the light shield such that the light shield is disposed between the first and second **passivation layers**. The **passivation layers** and the light shield define openings above each of the plurality of **bond** pads that allow an upper bump pad to be disposed on the **bonding** pads, and a solder bump to be disposed on the upper bump pad. The solder bumps are used to couple the integrated circuit to a substrate, such as a printed circuit board.
RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 2 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:648284 HCAPLUS
DN 139:172333
TI Design and fabrication of a transformer containing stacked inductors
IN Fazelpour, Siamak
PA Skyworks Solutions, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6608363	B1	20030819	US 2001-797307	20010301

PRAI US 2001-797307 20010301
AB The invention relates to the design and fabrication of a transformer containing stacked inductors. The transformer consists of (i) an inductor fabricated over a **bond** pad, where the inductor is elec. connected to the **bond** pad; (ii) a dielec. deposited over the inductor; (iii) a second inductor fabricated over the dielec., where the second inductor is cross-coupled with the first inductor. The first inductor, the dielec., and the second inductor are all encapsulated in a package.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 3 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:319220 HCAPLUS
DN 138:330088
TI Wire **bond** structure and method to connect to a microelectronic die
IN Gleixner, Robert J.; Danielson, Donald; Paluda, Patrick M.; Naik, Rajan
PA Intel Corporation, USA
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003075804	A1	20030424	US 2001-32623	20011018
	US 6683383	B2	20040127		
	WO 2003056625	A2	20030710	WO 2002-US33568	20021017
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
	US 2003205827	A1	20031106	US 2003-454979	20030605
PRAI	US 2001-32623	A	20011018		

AB The present invention relates generally to microelectronic dies and packaging such devices, and more particularly to a wire **bond** structure and method to make an elec. connection to a microelectronic die. A wire **bond** structure includes a Cu pad formed on or in a surface of a microelectronic die. A conductive layer is included in contact with the Cu pad and a **bond** wire is **bonded** to the conductive layer. The conductive layer is formed of a material to provide a stable contact between the **bond** wire and the Cu pad in at least one of an oxidizing environment and an environment with temps. up to at least .apprx.350°.

L17 ANSWER 4 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:196931 HCAPLUS
DN 138:213600
TI Method of forming a **bond** pad in a semiconductor device
IN Kobayashi, Thomas S.; Pozder, Scott K.
PA Motorola, Inc., USA

SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6531384	B1	20030311	US 2001-952527	20010914
US 2003054626	A1	20030320		
PRAI US 2001-952527		20010914		

AB The invention relates to a method of forming a **bond** pad in a semiconductor device. A **bond** pad is formed by first providing a planarized combination of copper and **silicon oxide** features in a **bond** pad region. The **silicon oxide** features are etched back to provide a plurality recesses in the copper in the **bond** pad region. A corrosion barrier is formed over the copper and the **silicon oxide** features in the recesses. Probing of the wafer is done by directly applying the probe to the copper. A wire **bond** is directly attached to the copper. The presence of the features improves probe performance because the probe is likely to slip. Also, the probe is prevented from penetrating all the way through the copper because the recessed features are present. With the recesses in the copper, the wire **bond** more readily breaks down and penetrates the corrosion barrier and is also less likely to slip on the **bond** pad.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 5 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:978223 HCAPLUS
DN 138:41459
TI Structure and method for improved **adhesion** between two polymer films
IN Egitto, Frank D.; Matienzo, Luis J.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002195197	A1	20021226	US 2001-878474	20010611
US 6656313	B2	20031202		
PRAI US 2001-878474		20010611		

AB A method for improving the **adhesion** between **polyimide** layers and the structure formed by the method. A **silicon oxide**-containing layer is formed on the surface of a **polyimide** layer and a second layer of **polyimide** is formed on the **silicon oxide**-containing layer. The materials are suitable as protective **coatings** for semiconductors, as **dielec. layers** for **multilayer** integrated circuits, as high-temperature solder masks, as **bonding** for multilayer circuits, and as the final **passivation coating** on electronic devices.

L17 ANSWER 6 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:676345 HCAPLUS
DN 137:225230

TI Method of forming a notched silicon-containing gate structure
IN Yang, Chan-Syun David; Shen, Meihua; Yauw, Oranna; Chinn, Jeffrey D.
PA Applied Materials, Inc., USA
SO PCT Int. Appl., 58 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002069383	A2	20020906	WO 2002-US2318	20020125
	WO 2002069383	A3	20030206		
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
	US 2002151183	A1	20021017	US 2001-791446	20010222
	US 6551941	B2	20030422		
PRAI	US 2001-791446	A	20010222		

AB The present invention pertains to a method of forming a notched silicon-containing gate structure. In particular, the present invention provides a multiple step method of forming a notched silicon-containing gate structure which provides good control over notch dimensions and excellent notch dimension uniformity across the surface of a substrate. This method is particularly useful in forming a T-shaped Si-containing gate structure. A Si-containing gate layer is etched to a 1st desired depth using a plasma generated from a 1st source gas. During the etch, etch by products deposit on upper sidewalls of the Si-containing gate layer which are exposed during etching, forming a 1st **passivation layer** which protects the upper Si-containing gate layer sidewalls from etching during subsequent processing steps. A relatively high substrate bias power is used during this 1st etch step to ensure that the **passivation layer adheres** properly to the upper Si-containing gate sidewalls. The remaining portion of the Si containing gate layer is etched at a lower bias power using a plasma generated from a 2nd source gas which selectively etches the Si-containing gate layer relative to the underlying gate **dielec. layer**, whereby a lower sidewall of the Si-containing gate layer is formed and an upper surface of the gate **dielec. layer** is exposed. The etch stack is then exposed to a plasma generated from a 3rd source gas which includes N, whereby a 2nd, N-containing **passivation layer** is formed on the exposed sidewalls of the Si-containing gate layer. Subsequently, a notch is etched in the lower sidewall of the Si-containing gate layer. Subsequently, a notch is etched in the lower sidewall of the Si-containing gate layer. The method of the invention provides control over both the height and the width of the notch, while providing a marked improvement in notch critical dimension uniformity between isolated and dense feature areas of the substrate.

L17 ANSWER 7 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:221123 HCAPLUS
DN 136:255748
TI Micro c-4 semiconductor die and method for depositing connection sites thereon
IN Farrar, Paul A.; Eldridge, Jerome
PA USA
SO U.S. Pat. Appl. Publ., 16 pp., Cont.-in-part of U. S. Ser. No. 546,084.
CODEN: USXXCO
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002034581	A1	20020321	US 2001-773522	20010202
	US 2002034582	A1	20020321	US 2001-960104	20010921
	US 6491969	B2	20021210		
	US 2003186485	A1	20031002	US 2003-396558	20030326
	US 2003183677	A1	20031002	US 2003-396571	20030326
PRAI	US 2000-546084	A2	20000410		
	US 2001-773522	A3	20010202		

AB A semiconductor die having multiple solder bumps, each having a diameter .ltorsim.100 μm, and the method for making such a die are described. The solder bumps are preferably .apprx.10 μm in diameter, and the pitch between the solder bumps is <100 μ, and preferably less than or equal to 10 μ. A thermal solder jet apparatus is used to deposit solder material to form the solder bumps. The apparatus includes a print head having a plurality of solder ejection ports. Each ejection port has an associated gas ejection conduit connected to a chamber containing ≥1 hydride films. The hydride film is heated to dissociate H gas. The H gas rapidly builds up in the conduit which leads to the ejection port which is loaded with a solder material and forces the ejection of the solder material from the port. A controller controls and choreographs the movements of the movable substrate and movable drive so as to accurately deposit material in desired locations on the semiconductor dies.

L17 ANSWER 8 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:703763 HCAPLUS
DN 135:235008
TI Process for controlling oxide thickness over a fusible link using transient etch stops
IN Tzeng, Wen-Tsing; Chen, Yue-Feng; Wang, Kau-Jan
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6294474	B1	20010925	US 1999-425906	19991025
PRAI	US 1999-425906		19991025		

AB A method is described for progressively forming a fuse access opening for laser trimming in an integrated circuit with improved control of dielec. thickness over the fuse. A **dielec. layer** is formed over the fuse and a polysilicon layer is then patterned over the fuse to form a 1st etch stop. An inter-level **dielec.** (ILD) **layer** is added and a 2nd etch stop is formed in a 1st metal layer on the ILD layer over the 1st etch stop. The 2nd etch stop serves to protect the ILD layer over the fuse from being etched by an ARC over etch during the via etching in a 1st inter-metal **dielec.** (IMD) **layer**. A 1st portion of the laser access window is formed during the via etching of the 1st IMD layer. The 2nd etch stop is then removed by the 2nd metal patterning etch, exposing the ILD layer over the 1st etch stop at it's original thickness. A **passivation layer** is deposited and patterned to form access openings to **bonding** pads as well as to further open the laser access window to the 1st etch stop. The 1st etch stop prevents penetration of the subjacent **insulative layer** over the fuse, thereby maintaining a

controlled uniform thickness of that layer. When the **bonding** pads are opened, including the removal of an ARC on their surface, the etchant conditions are changed to remove the etch stop and subsequently a portion of the subjacent **insulative layer** over the fuse leaving a precise and uniform thickness of dielec. material over the fuse. The process fits conveniently within the framework of an existing process and does not introduce any addnl. steps.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 9 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:352276 HCAPLUS
DN 134:347174
TI Method for preventing corrosion of **bonding** pad on a surface of a semiconductor wafer
IN Chang, Yi-chun; Chen, Jain-hon
PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6232238	B1	20010515	US 1999-264012	19990208
PRAI US 1999-264012		19990208		

AB The present invention provides a method for preventing corrosion of a **bonding** pad resulting from residual polymers on a surface of a semiconductor wafer. The **bonding** pad is a metallic layer formed on the surface of the semiconductor wafer. The semiconductor wafer comprises an inorg. **passivation layer** positioned above the **bonding** pad, and an organic **dielec. layer** positioned above the inorg. **passivation layer**. The **passivation** and **dielec. layers** comprise a hole etched to the **bonding** pad. The method uses an organic solution to clean off residual polymers on the surface of the **bonding** pad inside the hole to prevent corrosion of the **bonding** pad.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 10 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:73502 HCAPLUS
DN 134:124771
TI **Passivation layer** etching process for memory arrays with fusible links
IN Tzeng, Wen-Tsing; Yang, Chun-Pin; Lin, Hsing-Lien
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6180503	B1	20010130	US 1999-354852	19990729
PRAI US 1999-354852		19990729		

AB A method is described for progressively forming a fuse access openings in integrated circuits which are built with redundancy and use laser trimming

to remove and insert circuit sections. The fuses are formed in a polysilicon layer and covered by ≥1 relatively thin **insulative layers**. An etch stop is patterned over the fuse in a higher level polysilicon layer or a 1st metalization layer. Addnl. **insulative layers** such as inter-metal **dielec. layers** are then formed over the etch stop. A 1st portion of the laser access window is then etched during the via etch for the top metalization level. The etch stop prevents removal of the insulation subjacent to it. Cumulative thickness non-uniformities in the relatively thick upper **insulative layers** are thus removed from the fuse window. The etch stop is removed during patterning of the top level metalization. A **passivation layer** is applied and patterned to exposed **bonding** pads and, at the same time complete the etching of the laser access window to a desired thickness over the fuses. The **passivation layer** over etch required to penetrate the **insulation layer** over the fuses also removes an antireflective coating over the **bonding** pads. The process fit conveniently within the framework of an existing process and does not introduce any addnl. steps. In addition, the **passivation layer** can be patterned to form final access to both **bonding** pads and laser access openings with a single photolithog. mask.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 11 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:765537 HCAPLUS
DN 133:336006
TI Heat-resistant branched polymer compositions with low dielectric constant
IN Tomikawa, Masao; Fujiwara, Takenori
PA Toray Industries, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000302967	A2	20001031	JP 2000-36641	20000215
PRAI JP 1999-38472	A	19990217		

AB The compns., useful for **passivation films** and **interlayer insulation films**, contain polymers (A) containing 5-35 mol% C3-30 tri- or tetravalent crosslinking groups, solid particles (B), and tertiary amines (C), where A have structures selected from NHC:OQ1(CO2Q4)qC:ONH[Q2NHC:OQ3(CO2Q5)rC:O]pNH, NHC:OQ5C:O[NHQ7(ZH)tNHC:OQ8C:O]sNH, C:ONHQ9NHC:O[Q10(CO2Q12)vC:ONHQ11NHC:O]u, and C:ONHQ13(ZH)xNH[C:OQ14C:ONHQ15(ZH)yNH]wC:O (Q1,3,10 = C≥2 organic group with valence 3 or 4; Q2,6,8,9,11,14 = C≥2 organic group with valence 2; Q4,5,12, = H, C1-10 organic group with valence 1; Q3,5,7 = C≥2 organic group with valence 3-6; Z = O, S, NH; p, s, u, w = 1-100; q, r, t, v, x, y = 1, 2). Thus, a test piece manufactured from a polymer (prepared by polymerization of 3,4,4'-triaminodiphenyl ether, pyromellitic anhydride, and 2,2'-dimethyl-4,4'-diaminobiphenyl and addition of aniline and 3-aminopropyltrimethoxysilane), FEP (PTFE-polypropylene sol), and lutidine showed dielec. constant 2.21, heat resistance 450°, and good scratch resistance and **adhesion** to a Si wafer.

L17 ANSWER 12 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 2000:636236 HCAPLUS
DN 133:216533
TI Fabrication of insulator substrate crack resistant semiconductor device that involves fewer steps
IN Umehara, Norito; Amagai, Masazumi
PA Texas Instruments Incorporated, USA
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6118183	A	20000912	US 1997-990481	19971215
PRAI JP 1996-354427	A	19961219		

AB To provide a type of semiconductor device with high resistance to cracks and having fewer manufacturing steps. Semiconductor device has a substrate having insulating base material mainly made of a thermoplastic **polyimide** resin. When heated to a temperature above the glass transition temperature, the surface of insulating base material made of thermoplastic **polyimide** resin melts and exhibits the properties of an **adhesive**. The **adhesive** layer is preferred for laminating the metal film for forming conductor pattern, and it is preferred for fixing semiconductor IC chip to insulating base material made of thermoplastic **polyimide** resin. When semiconductor IC chip is fixed on insulating base material made of thermoplastic **polyimide** resin, the two are brought into contact with each other under a prescribed pressure, and the atmospheric temperature is higher than the glass transition temperature for **bonding**. Frame made up of a metal lead frame is arranged on the periphery of the insulating base material for reinforcing insulating base material made of thermoplastic **polyimide** resin.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 13 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:468525 HCAPLUS
DN 131:96168
TI A novel passivation structure and its method of fabrication for integrated circuits
IN Bohr, Mark T.
PA Intel Corporation, USA
SO PCT Int. Appl., 28 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 9934442	A1	19990708	WO 1998-US26689	19981215

W: AL, AM, AT, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ, DE, DE, DK, DK, EE, EE, ES, FI, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES,

FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

	US 6143638	A	20001107	US 1997-1551	19971231
	US 2002064929	A1	20020530	US 1998-115418	19980714
	AU 9919172	A1	19990719	AU 1999-19172	19981215
	JP 2002500445	T2	20020108	JP 2000-526974	19981215
PRAI	US 1997-1551	A	19971231		
	WO 1998-US26689	W	19981215		

AB A novel passivation structure and its method of fabrication. According to the present invention a 1st **dielec. layer** (204) is formed upon a conductive layer formed over a substrate. The 1st **dielec. layer** (204) and the conductive layer are then patterned into a 1st dielec. capped interconnect (208) and a dielec. capped **bond** pad (206). Next, a 2nd **dielec. layer** is formed over and between the dielec. capped interconnect (206) and the dielec. capped **bond** pad (208). The top portion of the 2nd **dielec. layer** is removed so as to expose the dielec. capped **bond** pad (208) and the dielec. capped interconnect (206). A 3rd **dielec. layer** (218) is then formed over the exposed dielec. capped **bond** pad and the exposed dielec. capped interconnect and over the 2nd dielec.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 14 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:810925 HCAPLUS
DN 123:215764
TI Manufacture of an integrated circuit having a fuse element
IN Yoshizumi, Keiichi; Fukuda, Kazushi; Ariga, Seiichi; Ikeda, Shuji; Saeki, Makoto; Nagai, Kiyoshi; Hashiba, Soichiro; Nishihara, Shinji; Kanai, Fumiyuki
PA Hitachi, Ltd., Japan; Hitachi ULSI Engineering Corp.
SO U.S., 64 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5444012	A	19950822	US 1994-278073	19940720
	JP 07037988	A2	19950207	JP 1993-178676	19930720
PRAI	JP 1993-178676		19930720		

AB In depositing a Si oxide film which constitutes part of a final **passivation film** onto a **bonding** pad formed on an **interlayer insulating film**, the Si oxide deposition step is divided into 2 stages, and after the 1st deposition, the **bonding** pad is once exposed by etching, then the 2nd deposition is performed, whereby the Si oxide film which has thus been deposited in 2 stages is formed over a fuse element formed under the **interlayer insulating film**, while on the **bonding** pad is formed only the Si oxide film deposited in the 2nd stage. As a result, at the time of etching **polyimide**, Si nitride, and Si oxide successively to expose the **bonding** pad, there remains a sufficient thickness of **insulating film** between the bottom of the aperture formed and the fuse element. Thereafter, an elec. test is conducted while applying a probe to the **bonding** pad and, where required, the fuse element located under the aperture is cut.

L17 ANSWER 15 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:541673 HCAPLUS
DN 122:280004
TI Manufacture of semiconductor device
IN Yamamoto, Tomie; Mase, Koichi; Abe, Masayasu
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07058107	A2	19950303	JP 1993-203810	19930818
PRAI	JP 1993-203810		19930818		

AB The title manufacture for **passivation films** involves the following steps: (1) successively forming an inorg. **insulator film**, a **polyimide film**, and a photoresist on a metal wire; (2) opening a window in a **polyimide** film by etching after patterning the photoresists; (3) removing the photoresists; (4) dry-etching the inorg. **insulator film** by RIE (reactive ion etching) using the **polyimide** film as a mask; and (5) removing a fixed amount of surface layer of the **polyimide** film. The surface layer of the **polyimide** film may be removed by O plasma ashing. Since F-containing residues are removed by ashing, pad-corrosion is prevented and **adhesion** strength with a mold resin is improved.

L17 ANSWER 16 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:313778 HCAPLUS
DN 120:313778
TI Manufacture of multilayered circuit substrate
IN Kobarikawa, Takashi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06013754	A2	19940121	JP 1992-165945	19920624
PRAI	JP 1992-165945		19920624		

AB The substrate is manufactured by forming a Cu circuit pattern on an elec. insulated base substrate via a metal **adhesive** layer, oxidizing the exposed pattern to form a Cu oxide coating layer, applying a polyamic acid on the coated pattern, and curing to form a **polyimide** layer. Reaction between the Cu pattern and the **polyimide** layer was prevented.

L17 ANSWER 17 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1989:184285 HCAPLUS
DN 110:184285
TI Manufacture of semiconductor device with **passivation film**
IN Yamamoto, Jiro
PA NEC Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 63271939	A2	19881109	JP 1987-107396	19870428
PRAI JP 1987-107396		19870428		

AB The title manufacture comprises the steps of: (1) forming an inorg. **insulating film** on a semiconductor substrate having a device region; (2) forming a photosensitive organic film; (3) forming openings in the organic film; (4) etching the inorg. film using the organic film as a mask; (5) dividing the substrate into pellets without removing the organic film; and (6) mounting, **bonding**, and sealing with a resin. This method requires only 1 photolithog. process in formation of a **passivation film**.

L17 ANSWER 18 OF 18 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1985:409059 HCAPLUS
DN 103:9059
TI Amorphous silicon solar-cell modules
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 60018972	A2	19850131	JP 1983-126012	19830713
PRAI JP 1983-126012		19830713		

AB An amorphous Si solar-cell module uses a common flexible and heat-resistant base. An **insulating film** (amorphous Si or a Cr oxide) is placed on the base and a 2nd **insulating film** (**SiO2**, Al2O3, or Si3N4) on the 1st **insulating film**. Thus, a **polyimide** resin was coated on a stainless-steel base and an amorphous Si and **SiO2** layers were sputtered on the resin layer. A bottom electrode was sputtered, an amorphous p-i-n-type Si solar cell was formed, an In-Sn oxide top electrode was applied, and a **SiO2** coating was formed as a **passivation film**. The inorg. **insulating layer** improves the **adhesion** of base and solar cell.

L19 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:43067 HCAPLUS
DN 120:43067
TI Passivation schemes for copper/polymer thin-film interconnections used in multichip modules
AU Adema, Gretchen M.; Hwang, Lih Tyng; Rinne, A.; Turlik, Iwona
CS Cent. Microelectron., MCNC, Research Triangle Park, NC, 27709, USA
SO IEEE Transactions on Components, Hybrids, and Manufacturing Technology (1993), 16(1), 53-9
CODEN: ITTEDR; ISSN: 0148-6411
DT Journal
LA English
AB An investigation was conducted to examine the use of thin inorg. **dielec. films** as barrier **layers** between copper and **polyimide**. Emphasis was placed upon discovering the effectiveness of the barrier layers in preventing copper/**polyimide** interaction and determining its impact on the high frequency elec. performance of transmission line structures. The integrity of the inorg. **dielec. layers** as diffusion barriers for the copper was analyzed using TEM. These effects were studied by depositing thin layers of Si3N4, **SiO2**, and SiOxNy between chromium/copper/chromium lines and either Dow Benzocyclobutene or Dupont 2525 **polyimide**. Both sputtered Si3N4 and **PECVD** SiOxNy behaved as diffusion barriers which resulted in improved performance at very high frequencies over unprotected transmission lines. Copper diffused through the sputtered **SiO2** confirming that it is inadequate as a diffusion barrier for copper. Because the thickness of the inorg. **dielec. layers** was very small in proportion to the thickness of the polymer dielecs. employed, no difference in the effective dielec. constant was seen over the entire frequency range measured.

L19 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1993:203317 HCAPLUS
DN 118:203317
TI Passivation schemes for copper/polymer thin film interconnections used in multichip modules
AU Adema, Gretchen M.; Hwang, Lih Tyng; Rinne, Glenn A.; Turlik, Iwona
CS MCNC Cent. Microelectron., Research Triangle Park, NC, 27709, USA
SO Proceedings - Electronic Components & Technology Conference (1992), 42nd, 776-82
CODEN: PETCES
DT Journal
LA English
AB An investigation was conducted to examine the use of thin inorg. **dielec. films** as barrier **layers** between copper and **polyimide**. Emphasis was placed upon discovering the effectiveness of the barrier layers in preventing copper/**polyimide** interaction and determining its impact on the high frequency elec. performance of transmission line structures. The integrity of the inorg. **dielec. layers** as diffusion barriers for the copper was analyzed using TEM. These effects were studied by depositing thin layers of Si3N4, **SiO2**, and SiOxNy between chromium/copper/chromium lines and either Dow Benzocyclobutene or Dupont 2525 **polyimide**. Both sputtered Si3N4 and **PECVD** SiOxNy behaved as diffusion barriers which resulted in improved performance at very high frequencies over unprotected transmission lines. Copper diffused through the

sputtered **SiO2** confirming that it is inadequate as a diffusion barrier for copper. Because the thickness of the inorg. **dielec. layers** was very small in proportion to the thickness of the polymer dielecs. employed, no difference in the effective dielec. constant was seen over the entire frequency range measured.

L19 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1988:14594 HCAPLUS
DN 108:14594
TI Comparative effects of polyamide and **PECVD** silicon nitride as **passivating layers** on gallium arsenide power MESFET characteristics
AU Donzelli, G. P.; Gabbrielli, B.
CS Telettra S.P.A., Vimercate, Italy
SO Applied Surface Science (1987), 30(1-4), 95-9
CODEN: ASUSEE; ISSN: 0169-4332
DT Journal
LA English
AB Two different dielec. materials (polyamide and **PECVD** (**plasma-enhanced chem.-vapor-deposition**) Si,N4 were used as **passivation coatings** for GaAs powder (metal-semiconductor FETs). The devices were submitted to accelerated life tests to characterize the behavior of the **insulating layers** during the periods of storage. This characterization was made by measuring the most important elec. (d.c. and radio-frequency) parameters of the devices and controlling their time evolution. The most significant result of the expts. is that the Si3N4 passivated devices show a greater stability of their parameters at the end of the 2 following tests: a storage without bias (high-temperature storage) and under operating conditions (high-temperature operating test). The 3rd test, performed under reverse gate bias at high temperature, did not reveal any noticeable difference between the devices with both types of coatings.

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File 342:Derwent Patents Citation Indx 1978-04/200402
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*File 342: New prices as of 1/1/04 per Information Provider request.
See HELP RATES342
? S PN=US 6352940
? MAP PN/CT=
? MAP PN/CG=

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File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)
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*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run. See HELP NEWS 347 for details.
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200410
(c) 2004 Thomson Derwent
*File 350: New prices as of 1-1-04 per Information Provider request.
See HELP RATES350

Set	Items	Description
S1	16	S1:S2
S2	6	S1 AND (PASSIVAT????????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?))
S3	6	IDPAT (sorted in duplicate/non-duplicate order)
S4	6	IDPAT (primary/non-duplicate records only)
S5	10	S1 NOT S2
S6	5	S5 AND (INSULAT?????? OR DIELECTR??????)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S7	5	IDPAT (sorted in duplicate/non-duplicate order)
S8	4	IDPAT (primary/non-duplicate records only)
S9	5	S5 NOT S6
S10	5	IDPAT (sorted in duplicate/non-duplicate order)
S11	5	IDPAT (primary/non-duplicate records only)

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4/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013144897
WPI Acc No: 2000-316769/**200027**
XRAM Acc No: C00-095704
XRPX Acc No: N00-237763
Passivating integrated circuit comprises depositing silicon nitride over a top surface portion of the circuit, and treating the exposed surface to form silicon oxynitride
Patent Assignee: INTEL CORP (ITLC)
Inventor: DASS M L A; GAETA I; SESHAN K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6046101	A	20000404	US 971970	A	19971231	200027	B

Priority Applications (No Type Date): US 971970 A 19971231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6046101	A		13	H01L-021/318	

Abstract (Basic): **US 6046101** A
Abstract (Basic):
NOVELTY - Integrated circuit is passivated by depositing a silicon nitride layer over the top surface of a portion of an integrated circuit, treating an exposed surface of the first **passivation layer** to form a silicon oxynitride layer and depositing a second passivation **layer** over the first **passivation layer**.
USE - For passivating integrated circuit.
ADVANTAGE - Delamination is minimized by eliminating passivation material from the scribe street area prior to separating devices and the combined passivation technology has robust **passivation** resistance to thin **film** delamination.
pp; 13 DwgNo 0/21

4/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012103242
WPI Acc No: 1998-520154/**199844**
XRAM Acc No: C98-156147
XRPX Acc No: N98-406252
Forming a semiconductor IC with patterned polyimide passivation - including an oxygen plasma ashing step to remove residual polyimide from bond pads followed by a thermal treatment to restore low surface leakage current.
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: CHAO Y; FU W; LAN H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5807787	A	19980915	US 96755862	A	19961202	199844	B

Priority Applications (No Type Date): US 96755862 A 19961202
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

US 5807787 A 8 H01L-021/4762

Abstract (Basic): US 5807787 A

Polyimide passivation is formed on a semiconductor IC by: depositing a top insulation layer on the IC; etching contact openings; forming bond pads (4) in the openings; adding a first **passivation layer** (12); forming openings (6) in the layer to the bond pads (4); spin **coating** a second **passivation layer** (14) of polyimide; removing the layer over the bond pads and over the second **passivation layer** between the bond pads; plasma ashing in O2 to remove residual polyimide from the bond pads, which also causes an increase in surface leakage current on the first **passivation layer** (12) between the bond pads (4); and thermally treating to eliminate the increase and provide polyimide passivation on the IC with reduced surface leakage current between bond pads.

ADVANTAGE - The thermal treatment step eliminates the increased leakage current between the bond pads which results from the plasma ashing step. Leakage current is preferably reduced from about 1.0-2.0nA to about 0.1-0.2nA.

Dwg.3/3

4/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012049785
WPI Acc No: 1998-466695/**199840**
XRAM Acc No: C98-141485
XRPX Acc No: N98-363556

Passivation layer formation over spaced metal lines on semiconductor substrates - by sequentially forming plasma enhanced silicon nitride, silicon oxide and second silicon nitride layers

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: CHENG Y; YU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5795833	A	19980818	US 96691080	A	19960801	199840	B

Priority Applications (No Type Date): US 96691080 A 19960801
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5795833	A		6	H05H-001/24	

Abstract (Basic): US 5795833 A

A method of making **passivation layers** over spaced metal lines (20) over a semiconductor structure comprises forming the metal lines having a height of 0.4-0.8 microns, a width of 0.5-1.5 microns and a spacing of 0.5-1.0 microns and forming a silicon nitride layer (24) 900-1000 Angstrom thick by plasma enhanced chemical vapour deposition) PECVD. This is followed by a silica layer (28) 4000-9000 Angstrom thick, formed by PECVD using a flow of O2, TEOS and N2, each at a flow rate of 900-1100 mg per minute, a pressure of 7.2-9.2 torr, a deposition temperature of 390-410 deg. C, an rf power of 650-775 W and an electrode gap of 220-280 mils.

A second silicon nitride layer (32), 4000-7000 Angstrom thick, is then formed by PECVD. Preferably an insulating layer of polyimide or epoxy is formed over the second nitride layer.

USE - In forming **passivation layers** over metal lines in

semiconductor integrated circuits.
ADVANTAGE - The barrier is moisture-proof, step coverage is good and stress between the lines and overlying layers is reduced.
Dwg.2/2

4/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009823412
WPI Acc No: 1994-103268/**199413**
XRAM Acc No: C94-047551
Hermetically sealed IC - includes a PVD or CVD ceramic sealing layer which also covers the sidewalls of a prim. **passivation layer** and bond pad and street sites
Patent Assignee: MICHAEL K W (MICH-I); DOW CORNING CORP (DOWO)
Inventor: MICHAEL K W; KEITH WINTON M
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 589678	A2	19940330	EP 93307461	A	19930921	199413	B
CA 2106694	A	19940324	CA 2106694	A	19930922	199423	
JP 6204282	A	19940722	JP 93236014	A	19930922	199434	
TW 232095	A	19941011	TW 93107683	A	19930920	199445	
EP 589678	A3	19950412	EP 93307461	A	19930921	199544	
US 5825078	A	19981020	US 92948570	A	19920923	199849	

Priority Applications (No Type Date): US 92948570 A 19920923
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 589678	A2	E	6	H01L-023/02	
Designated States (Regional): DE FR GB IT NL					
JP 6204282	A		5	H01L-021/60	
CA 2106694	A			H01L-023/29	
TW 232095	A			H01L-023/28	
EP 589678	A3			H01L-023/02	
US 5825078	A			H01L-023/58	

Abstract (Basic): EP 589678 A
IC comprises: a circuit assembly with bond pads; a prim. **passivation layer** which is etched at the bond pads and streets; and one more ceramic **layers** covering the prim. **passivation layer** including the sidewalls created by etching at the pads and streets, the ceramic layer(s) being PVD or CVD layers.
A non-corroding conductive layer, pref. of Au, Ag, W, solder, Cu or Ag-filled epoxy, is included on the bond pads. A diffusion barrier layer on the pads may also be included. The ceramic layer(s) are formed of ceramics based on Si, SiO, SiN, SiON, SiOC, SiCN, SiOCN, SiC or diamond-like C materials. The diffusion barrier layer is pref. Ti, TiW or TiN. The device may be encapsulated in an organic or silicone encapsulant.
ADVANTAGE - The PVD or CVD ceramic layer(s) provide sealing of enhanced hermeticity esp. at the pads and streets.
Dwg.0/2

4/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002038572
WPI Acc No: 1978-51621A/**197828**
Crack resistant passivating overcoat for semiconductor device - of glass and low temp. deposited non-stoichiometric silicon nitride
Patent Assignee: RCA CORP (RADC)
Inventor: LEWIS W N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4091406	A	19780523				197828 B

Priority Applications (No Type Date): US 76737848 A 19761101

Abstract (Basic): US 4091406 A

A semiconductor device having a primary **passivating layer** of insulating material, including an Si3N4 layer, on the semiconductor and a metallic conductor on the insulator has a passivating overcoat including (a) a glass layer on the conductor and (b) a low temp. deposited nitride layer of SiwNxHyOz on the glass, where w, x, y, z are integers is not = 0. The nitride layer is deposited at < eutectic temp. at which the metallic conductor begins to alloy with the semiconductor.

The comination glass/nitride overcoat exhibits improved resistance to cracking, increasing device reliability. It seals the glass from ambient air, reducing degradation in adherence to the underlying metal

4/3,AB/6 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

06099152
PROCESS FOR FORMING SEMICONDUCTOR DEVICE

PUB. NO.: 11-040671 A]
PUBLISHED: February 12, 1999 (19990212)
INVENTOR(s): JAIN AJAY
APPLICANT(s): MOTOROLA INC
APPL. NO.: 10-202766 [JP 98202766]
FILED: July 02, 1998 (19980702)
PRIORITY: 895017 [US 895017], US (United States of America), July 16, 1997 (19970716)

ABSTRACT

PROBLEM TO BE SOLVED: To make a strong contact generate between a compound copper layer and a diffusion barrier film by transferring a part of an insulating layer which is made patterning into the barrier film, by adhering a contact layer on the barrier film and by forming a conductive metal containing layer on the contact layer.

SOLUTION: A second insulating layer is formed on a substrate 12 and a mutual junction 28. Next a dual in lay apperture is formed by patterning the insulating layer. Next an exposed surface of on oxide film 26 is transferred to a silicon oxy-nitride diffusion barrier part 56 by performing a plasma nitride step. After that a silicon contact layer 58 is formed on the barrier part 56. After a copper seed layer is adhered on the insulating layer, a compound copper layer which lies on the contact layer 58 is formed by performing an electrical plating processing. Further a dual

in lay constriction 74 including a via part and a mutual functioning channel part is formed by eliminating the parts of the contact layer 58 and the compound copper layer by chemical machining polishing. After that a **passivation layer** 66 is formed on a semiconductor device 68 including the structure 74.

8/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012527088
WPI Acc No: 1999-333194/**199928**
Related WPI Acc No: 2002-224448
XRAM Acc No: C99-098470
XRPX Acc No: N99-250824
Dielectric gate forming method for MOSFET - involves exposing semiconductor substrate to oxygen and nitrogen content gases to predetermined period to form oxy nitride gate **dielectric layers**
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: HEGDE R I; O'MEARA D; TOBIN P J; TSENG H; WANG V
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11121453	A	19990430	JP 98231211	A	19980803	199928	B
US 5972804	A	19991026	US 97906509	A	19970805	199952	
			US 97963436	A	19971103		
KR 99023305	A	19990325	KR 9831471	A	19980803	200024	
TW 408431	A	20001011	TW 98111051	A	19980708	200116	

Priority Applications (No Type Date): US 97963436 A 19971103; US 97906509 A 19970805
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11121453	A		17	H01L-021/318	
US 5972804	A			H01L-021/285	CIP of application US 97906509
KR 99023305	A			H01L-021/3205	
TW 408431	A			H01L-021/76	

Abstract (Basic): JP 11121453 A
NOVELTY - A semiconductor substrate is exposed to nitrogen content gas for predetermined period and then to oxygen content gas. Oxy nitride gate **dielectric films** with ratio of oxygen and nitrogen along thickness of **dielectric layers** varying with time are formed.
USE - For MOSFET in integrated circuits.
Dwg.2/20

8/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012150781
WPI Acc No: 1998-567693/**199848**
XRAM Acc No: C98-170593
XRPX Acc No: N98-441621
Semiconductor device with inlaid interconnects - of a strongly adhered composite copper material
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: JAIN A
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5821168	A	19981013	US 97895017	A	19970716	199848	B
JP 11040671	A	19990212	JP 98202766	A	19980702	199917	

KR 99013826 A 19990225 KR 9828278 A 19980714 200018

Priority Applications (No Type Date): US 97895017 A 19970716
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5821168	A		10	H01L-021/00	
JP 11040671	A		8	H01L-021/768	
KR 99013826	A			H01L-021/30	

Abstract (Basic): US 5821168 A

A semiconductor device is formed by forming a patterned **insulating layer**, including an opening, over a substrate. A portion of the patterned **insulating layer** is converted to a barrier film, and an adhesion layer deposited over it. A conductive metal-containing layer is formed over the adhesion layer.

USE - Processes for forming semiconductor devices with inlaid interconnects.

ADVANTAGE - The process does not require a separate diffusion barrier, the adhesion layer is formed such that it can react with the copper-containing interconnecting material resulting in strong adhesion between the composite copper layer and the diffusion barrier film, as well as to allow a more continuous interconnect and via structure that is more resistant to electromigration.

Dwg.1/10

8/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010188028
WPI Acc No: 1995-089281/**199512**
Related WPI Acc No: 1995-268922
XRAM Acc No: C95-040543
XRPX Acc No: N95-070603

Trench isolation structure in an integrated circuit - with improved reliability by increasing the thickness of the gate dielectric overlying the trench corner

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: POON S S; TSENG H
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5387540	A	19950207	US 93130052	A	19930930	199512	B
EP 646956	A2	19950405	EP 94114087	A	19940908	199518	
JP 7115124	A	19950502	JP 94251545	A	19940921	199526	
EP 646956	A3	19970709	EP 94114087	A	19940908	199740	
SG 45265	A1	19980116	SG 962288	A	19940908	199811	
KR 306935	B	20011201	KR 9424238	A	19940927	200247	
EP 646956	B1	20030129	EP 94114087	A	19940908	200309	
DE 69432068	E	20030306	DE 632068	A	19940908	200325	
			EP 94114087	A	19940908		

Priority Applications (No Type Date): US 93130052 A 19930930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5387540	A	E	11	H01L-021/76	
EP 646956	A2	E	11	H01L-021/76	
Designated States (Regional): DE FR GB IT					
JP 7115124	A		7	H01L-021/76	

EP 646956 A3 H01L-021/76
SG 45265 A1 H01L-021/76
KR 306935 B H01L-021/76 Previous Publ. patent KR 95010019
EP 646956 B1 E H01L-021/76
Designated States (Regional): DE FR GB IT
DE 69432068 E H01L-021/76 Based on patent EP 646956

Abstract (Basic): US 5387540 A

Forming a trench isolation structure in an IC comprises: providing a semiconductor substrate, the substrate having a trench isolation region and an active region formed therein, the trench isolation regions abutting the active region to form a trench corner; forming a first **dielectric layer** overlying the active region; wherein the first **dielectric layer** is formed only on the active region and abuts the trench corner; forming a second **dielectric layer** overlying the trench corner, wherein the first and second **dielectric layers** form a gate **dielectric layer**, the gate **dielectric layer** having a thickness is less than 20nm; forming a transistor gate electrode overlying the trench corner, wherein the gate **dielectric layer** lies between the trench corner and the transistor gate electrode.

USE - Formation of a trench isolation structure in an IC.

ADVANTAGE - Allows high density ICs to be fabricated with improved reliability due to increased breakdown voltage of the gate dielectric.

Dwg.10/15

8/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010107022
WPI Acc No: 1995-008275/**199502**
XRAM Acc No: C95-003033
XRPX Acc No: N95-006875
Semiconductor devices mfg. method - provides improved adhesion between **dielectric layers** at their interface
Patent Assignee: SGS THOMSON MICROELTRN SRL (SGSA); SGS THOMSON MICROELTRN SARL (SGSA)
Inventor: BACCHETTA M; BACCI L; ZANOTTI L
Number of Countries: 006 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 627763	A1	19941207	EP 93830243	A	19930531	199502	B
JP 7142730	A	19950602	JP 94139620	A	19940531	199531	
US 5627403	A	19970506	US 94235173	A	19940428	199724	
			US 95473552	A	19950606		
US 5795821	A	19980818	US 94235173	A	19940428	199840	
			US 96751244	A	19961118		

Priority Applications (No Type Date): EP 93830243 A 19930531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 627763	A1	E	8	H01L-021/316	
Designated States (Regional): DE FR GB IT					
JP 7142730	A		7	H01L-029/78	
US 5627403	A		6	H01L-021/471	Div ex application US 94235173
US 5795821	A			H01L-021/318	Cont of application US 94235173

Abstract (Basic): EP 627763 A

A method for improved adhesion between **dielectric** material **layers** at the interface thereof, during the mfr. of a semiconductor device, comprising operations for forming a first **layer** of a **dielectric** material (1) over at least a portion of a structure (7) defined on a substrate of a semiconductor material (6) and subsequently forming a second **layer** (3) of **dielectric** material overlying at least a portion of the first layer (1), characterised in that a thin oxide layer (2) is formed at least in one region between the first **layer** of **dielectric** material and the second, in contact with both.

Dwg.1/1

Abstract (Equivalent): US 5627403 A

An integrated circuit, comprising: a substrate of a semiconductor material; a first patterned conductor layer formed over the substrate; a dielectric; and a second upper patterned conductor **layer**; where the **dielectric** comprises: a first **layer** of a first silicon nitride compound; a thin silicon dioxide layer in contact with the first layer of the first silicon nitride compound at least in a region; and a second layer of a second silicon nitride compound overlaying the first layer of the first silicon nitride compound at least in the region and in contact with the thin silicon dioxide layer at least in the region; the thickness of the thin silicon dioxide being less than both the thicknesses of the first and second layers of the first and second silicon nitride compounds where the thickness of the thin silicon dioxide layer is in the range between 5 and 50 nm.

Dwg.2/2

11/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012150785
WPI Acc No: 1998-567697/**199848**
XRAM Acc No: C98-170597
XRPX Acc No: N98-441625
MOS gate dielectric with nitrogen incorporated at the substrate interface - using a process with increased oxidation rate resulting in a higher concentration of nitrogen
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: GARDNER M I; GILMER M C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5821172	A	19981013	US 97779264	A	19970106	199848	B

Priority Applications (No Type Date): US 97779264 A 19970106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5821172	A		7	H01L-021/322	

Abstract (Basic): US 5821172 A

A transistor is fabricated by; (a) Immersing a silicon monocrystalline substrate with a resistivity of 10 - 15 Omega .cm in an oxidation chamber at 400 - 700 deg. C (preferably 600 - 700 deg. C) and containing N2 or Ar, and 1 - 10% O2, to form a base layer of oxide substantially devoid of nitrogen. (b) Ramping the temperature to 600 - 1100 deg. C and simultaneously introducing NH3 and NO or N2O to form an oxynitride layer on the upper surface of the oxide. (d) Forming a conductive gate layer on the oxynitride layer. (e) Introducing source / drain impurity regions laterally displaced on either side of a channel region aligned with the gate.

USE - MOS transistors.

ADVANTAGE - The improved process has an increased oxidation rate which results in a higher nitrogen concentration in the dielectric. Penetration of boron from the conductive gate into the channel is reduced and dielectric reliability improved.

Dwg.1/2

11/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011970116
WPI Acc No: 1998-387026/**199833**
Related WPI Acc No: 1996-208836
XRAM Acc No: C98-116997
XRPX Acc No: N98-301810
Manufacture of an insulated gate field effect transistor, e.g. a TFT for a liquid crystal display - in which the gate insulation is a chlorine-containing silicon oxynitride layer with maximum nitrogen concentration at the interface with the gate electrode
Patent Assignee: SEMICONDUCTOR ENERGY LAB (SEME)
Inventor: TERAMOTO S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

US 5773325 A 19980630 US 94261920 A 19940616 199833 B
US 96598279 A 19960208

Priority Applications (No Type Date): US 94261920 A 19940616; US 96598279 A 19960208
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 5773325 A 12 H01L-021/318 Div ex application US 94261920
Div ex patent US 5508532

Abstract (Basic): US 5773325 A
An insulated gate field effect semiconductor device is formed with SiOxNy added with chlorine as gate insulation deposited from a precursor gas mixture containing (di)chlorosilane (x is 0-2, y is 0-4/3). The N concentration in the film is graded so that it is greatest at the interface with the gate electrode.
USE - For TFT fabrication for a liquid crystal display device or image sensor.
ADVANTAGE - By providing a high N concentration at the gate electrode interface, the diffusion of H and other ions into the gate is prevented. The Cl in the film suppresses the effects of moveable ions such as Na and heavy metals.
Dwg.3b,6/8

11/3,AB/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04850130
BOUNDARY ADHESION METHOD BETWEEN INSULATION MATERIALS

PUB. NO.: 07-142730 [**JP 7142730** A]
PUBLISHED: June 02, 1995 (19950602)
INVENTOR(s): MAURITSUIO BATSUKETSUTA
RAURA BATSUCHI
RUKA TSUANOTSUTEI
APPLICANT(s): SGS THOMSON MICROELETTRONICA SPA [197090] (A Non-Japanese Company or Corporation), IT (Italy)
APPL. NO.: 06-139620 [JP 94139620]
FILED: May 31, 1994 (19940531)
PRIORITY: 93830243 [EP 93830243], EP (European Patent Office), May 31, 1993 (19930531)

11/3,AB/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04822524
TRENCH SEPARATION STRUCTURE AT INSIDE OF INTEGRATED CIRCUIT AND FORMATION METHOD

PUB. NO.: 07-115124 [**JP 7115124** A]
PUBLISHED: May 02, 1995 (19950502)
INVENTOR(s): SUTEIIBUN ESU PUUN
SHIN FUAN TSUEN
APPLICANT(s): MOTOROLA INC [000782] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 06-251545 [JP 94251545]

FILED: September 21, 1994 (19940921)
PRIORITY: 7-130,052 [US 130052-1993], US (United States of America), September 30, 1993 (19930930)

11/3,AB/5 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

04733282
HERMETICALLY-SEALED INTEGRATED CIRCUIT

PUB. NO.: 06-204282 [**JP 6204282** A]
PUBLISHED: July 22, 1994 (19940722)
INVENTOR(s): KEISU UINTON MITSUSHIERU
APPLICANT(s): DOW CORNING CORP [000738] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 05-236014 [JP 93236014]
FILED: September 22, 1993 (19930922)
PRIORITY: 7-948,570 [US 948570-1992], US (United States of America), September 23, 1992 (19920923)

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File 350:Derwent WPIX 1963-2004/UD,UM &UP=200410
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*File 350: New prices as of 1-1-04 per Information Provider request. See HELP RATES350
File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)
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*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2003/Nov
(c) 2003 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
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*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	565	AU=(SESHAN, K? OR SESHAN K?)
S2	61	AU=(DASS, M? OR DASS M?)
S3	240	AU=(BAKKER, G? OR BAKKER G?)
S4	7	S1 AND S2
S5	2	S4 AND S3
S6	5	S4 NOT S5
S7	5	RD (unique items)
S8	5	IDPAT (sorted in duplicate/non-duplicate order)
S9	857	S1:S3
S10	11	S9 AND PASSIVAT????????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S11	2	S10 AND (PLASMA()ENHANC?()CHEMICAL()VAPOR()DEPOSITION OR PECVD)
S12	9	S10 NOT S11
S13	9	RD (unique items)

5/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015780819
WPI Acc No: 2003-843021/200378
Related WPI Acc No: 2002-545919
XRAM Acc No: C03-236802
XRPX Acc No: N03-673656
Passivation of integrated circuit involves sequentially forming insulation layer, adhesion layer, and passivation layer on the integrated circuit
Patent Assignee: BAKKER G L (BAKK-I); DASS M L A (DASS-I); SESHAN K (SESH-I)
Inventor: **BAKKER G L; DASS M L A; SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020050629	A1	20020502	US 98105590	A	19980626	200378 B
			US 200113103	A	20011106	

Priority Applications (No Type Date): US 98105590 A 19980626; US 200113103 A 20011106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020050629	A1		18	H01L-023/58	Div ex application US 98105590

Abstract (Basic): US 20020050629 A1
Abstract (Basic):
NOVELTY - An integrated circuit is passivated by sequentially forming an insulation layer, an adhesion layer (150), and a first passivation layer (155) on the IC. The adhesion layer is formed by treating the surface of the insulating layer with a gas. The first passivation layer and the gas include a common element(s).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) A method of passivating a trench on a semiconductor substrate (26), comprising sequentially forming a trench(s), an insulating layer, an adhesion layer, and a first passivation layer;and
(b) A method of passivating spacers, comprising sequentially forming a spacer(s), an insulating layer, an adhesion layer, and a first passivation layer.
USE - For passivating ICs.
ADVANTAGE - The method improves the adhesion between oxides and the passivation layers, thus reducing the delamination that occurs during the manufacturing process of the devices such as thermal cycling and sawing.
DESCRIPTION OF DRAWING(S) - The figure shows the integrated circuit devices.
Substrate (26)
Adhesion layer (150)
First passivation layer (155)
Second passivation layer (160)
pp; 18 DwgNo 13/21

5/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014725215
WPI Acc No: 2002-545919/200258
Related WPI Acc No: 2003-843021
XRAM Acc No: C02-154711
XRPX Acc No: N02-432061
Passivation of integrated circuit devices for wire bond packaging, involves forming adhesion layer on surface of insulating layer by treating surface of insulating layer with gas
Patent Assignee: INTEL CORP (ITLC)
Inventor: **BAKKER G L; DASS M L A; SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352940	B1	20020305	US 98105590	A	19980626	200258	B

Priority Applications (No Type Date): US 98105590 A 19980626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352940	B1		17	H01L-021/31	

Abstract (Basic): US 6352940 B1
Abstract (Basic):
NOVELTY - An integrated circuit (IC) device is passivated by forming an insulating layer (28) on a substrate (26). An adhesion layer (150) is formed into the surface of the insulating layer by treating the surface of the insulating layer with a gas. A first passivation layer is formed on the adhesion layer. The first passivation layer and the gas include common chemical element(s).
USE - For passivation of IC devices used in wire bond packaging.
ADVANTAGE - The inventive method improves adhesion between insulating layer and hard passivation layers of integrated circuit devices to reduce delamination that occurs during the manufacturing process of these devices, such as thermal cycling and sawing.
DESCRIPTION OF DRAWING(S) - The figures show the inventive integrated circuit devices.
Substrate (26)
Insulating layer (28)
Adhesion layer (150)
pp; 17 DwgNo 9, 10/21

8/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015309631
WPI Acc No: 2003-370565/200335
Related WPI Acc No: 2001-069759
XRPX Acc No: N03-295530
Probe card for integrated circuit bond pad testing, has probing beams with first ends coupled to PCB and second ends extending from the sloped sidewall of the probe assembly
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; KARKLIN K D; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6515358	B1	20030204	US 97941795	A	19970930	200335	B
			US 2000651388	A	20000829		

Priority Applications (No Type Date): US 97941795 A 19970930; US 2000651388 A 20000829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6515358	B1		25	H01L-023/06	Div ex application US 97941795 Div ex patent US 6143668

Abstract (Basic): US 6515358 B1
Abstract (Basic):
NOVELTY - Probing beams (230) have their first ends coupled to the printed circuit board (210) and their second ends extending from the sloped sidewall of the probe assembly (220). The beams are divided into two sets, with each set of beams extending from the sidewall portion at corresponding angles relative to the horizontal plane.
USE - For testing bond pad of integrated circuit.
ADVANTAGE - Reduces or eliminates the need for periodic tweaking or positional adjustment of the probe feature position during the life of the probe card due to uniform mechanical stresses between probe layers, thus facilitating greater availability for testing procedures. Provides more consistent outtravel. Allows better scrubbing and better contact with the bond pad due to tighter distribution of tip lengths. Reduces mutual inductance in the probe assembly between the power/signal probes and their complementing ground probe. Maintains and repeats nominal probe to bond pad contact resistance below standard level to allow consistent, repeatable testing of integrated circuit devices, thus allowing a higher degree of re-sort repeatability.
DESCRIPTION OF DRAWING(S) - The figure shows the schematic planar cross-sectional view of the probe card.
Printed circuit board (210)
Probe assembly (220)
Probing beams (230)
pp; 25 DwgNo 20/24

8/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014676912
WPI Acc No: 2002-497969/200253
XRAM Acc No: C02-141137

XRPX Acc No: N02-394050
Wafer cutting apparatus for semiconductor chip manufacture detects variations in height of wafer to control motor and to vary the sawing of wafer in selected direction
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; GAETA I S; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6357330	B1	20020319	US 99227493	A	19990107	200253	B

Priority Applications (No Type Date): US 99227493 A 19990107
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6357330	B1		14	B23D-005/30	

Abstract (Basic): US 6357330 B1
Abstract (Basic):
NOVELTY - A detector (116) facing a surface of a wafer (114) provided on a wafer holder (136) detects the variations in height of the wafer along a selected direction. Based on the variations, a central control unit (118) controls motors (154,156) independently to vary the rotational speed of corresponding sawing blades (158,160) mounted on a spindle (157) to saw the wafer in the selected direction.
USE - For semiconductor chip manufacture.
ADVANTAGE - Wafer is effectively sawed based on the variations of the height of the wafer.
DESCRIPTION OF DRAWING(S) - The figure shows the wafer cutting apparatus.
Wafer (114)
Detector (116)
Central control unit (118)
Wafer holder (136)
Motors (154,156)
Spindle (157)
Sawing blades (158,160)
pp; 14 DwgNo 3/9

8/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595490
WPI Acc No: 2001-079697/200109
XRAM Acc No: C01-022842
XRPX Acc No: N01-060655
Test of an integrated circuit device for their functionality involves depositing a solder bump on a surface of a bond pad on an integrated circuit device, heat treating the solder bump, and testing the integrated circuit device
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6162652	A	20001219	US 971969	A	19971231	200109	B

Priority Applications (No Type Date): US 971969 A 19971231
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 6162652 A 13 H01L-021/66

Abstract (Basic): US 6162652 A
Abstract (Basic):
NOVELTY - An integrated circuit device is tested by depositing a solder bump (150) on a surface of a bond pad on an integrated circuit device, heat treating the solder bump to transform the surface of the bump from rough to smooth, and testing the integrated circuit device by probing the solder bump.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of preparing a solder bump for testing.
USE - For testing an integrated circuit device to evaluate their functionality.
ADVANTAGE - Allows designers to evaluate the functionality of new devices during development, testing reliability and functionality of each die on a wafer before incurring the higher costs of packaging, performance of the production process to be evaluated, and production consistency to be rated.
DESCRIPTION OF DRAWING(S) - The drawing shows a schematic illustration of the integrated circuit device showing the processing step of electrically testing the solder bump.
solder bump (150)
pp; 13 DwgNo 16/18

8/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013585552
WPI Acc No: 2001-069759/200108
Related WPI Acc No: 2003-370565
XRAM Acc No: C01-019292
XRPX Acc No: N01-052717
Method for exposing bond pad in integrated circuit having two passivation layers, involves removing portion of second passivation layer over bond pad, curing remaining second passivation layer and etching exposed first passivation layer
Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; KARKLIN K D; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6143668 A 20001107 US 97941795 A 19970930 200108 B

Priority Applications (No Type Date): US 97941795 A 19970930
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6143668 A 25 H01L-021/31
Abstract (Basic): US 6143668 A
Abstract (Basic):
NOVELTY - A bond pad (110) in an integrated circuit coated with first (120) and second (130) passivation layers is exposed by removing a portion of the second passivation layer over the bond pad, curing the remaining portions of the second passivation layer and etching the exposed first passivation layer to expose the bond pad.
USE - The method is used in fabrication of integrated circuit devices such as a probe card having a pad pitch of less than 80 micron.
ADVANTAGE - The method produces durable probe features with

reliable contacts to bond pads having a low pad pitch.

DESCRIPTION OF DRAWING(S) - The drawing shows a stage for removal of the first passivation layer.

Aluminum bond pad (110)

Hard passivation layer (120)

Photodefinable polyimide passivation layer (130)

Residual layer following the polyimide curing step (140)

pp; 25 DwgNo 14/24

8/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013144897

WPI Acc No: 2000-316769/200027

XRAM Acc No: C00-095704

XRPX Acc No: N00-237763

Passivating integrated circuit comprises depositing silicon nitride over a top surface portion of the circuit, and treating the exposed surface to form silicon oxynitride

Patent Assignee: INTEL CORP (ITLC)

Inventor: **DASS M L A**; GAETA I; **SESHAN K**

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6046101	A	20000404	US 971970	A	19971231	200027	B

Priority Applications (No Type Date): US 971970 A 19971231

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6046101	A		13	H01L-021/318	

Abstract (Basic): US 6046101 A

Abstract (Basic):

NOVELTY - Integrated circuit is passivated by depositing a silicon nitride layer over the top surface of a portion of an integrated circuit, treating an exposed surface of the first passivation layer to form a silicon oxynitride layer and depositing a second passivation layer over the first passivation layer.

USE - For passivating integrated circuit.

ADVANTAGE - Delamination is minimized by eliminating passivation material from the scribe street area prior to separating devices and the combined passivation technology has robust passivation resistance to thin film delamination.

pp; 13 DwgNo 0/21

11/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015780819
WPI Acc No: 2003-843021/200378
Related WPI Acc No: 2002-545919
XRAM Acc No: C03-236802
XRPX Acc No: N03-673656
Passivation of integrated circuit involves sequentially forming insulation **layer**, adhesion **layer**, and **passivation layer** on the integrated circuit
Patent Assignee: BAKKER G L (BAKK-I); DASS M L A (DASS-I); SESHAN K (SESH-I)
Inventor: **BAKKER G L; DASS M L A; SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020050629	A1	20020502	US 98105590	A	19980626	200378 B
			US 200113103	A	20011106	

Priority Applications (No Type Date): US 98105590 A 19980626; US 200113103 A 20011106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020050629	A1		18	H01L-023/58	Div ex application US 98105590

Abstract (Basic): US 20020050629 A1
Abstract (Basic):
NOVELTY - An integrated circuit is passivated by sequentially forming an insulation layer, an adhesion layer (150), and a first **passivation layer** (155) on the IC. The adhesion layer is formed by treating the surface of the insulating layer with a gas. The first **passivation layer** and the gas include a common element(s).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(a) A method of passivating a trench on a semiconductor substrate (26), comprising sequentially forming a trench(s), an insulating **layer**, an adhesion **layer**, and a first **passivation layer**;and
(b) A method of **passivating spacers**, comprising sequentially forming a spacer(s), an insulating **layer**, an adhesion **layer**, and a first **passivation layer**.
USE - For passivating ICs.
ADVANTAGE - The method improves the adhesion between oxides and the **passivation layers**, thus reducing the delamination that occurs during the manufacturing process of the devices such as thermal cycling and sawing.
DESCRIPTION OF DRAWING(S) - The figure shows the integrated circuit devices.
Substrate (26)
Adhesion layer (150)
First **passivation layer** (155)
Second **passivation layer** (160)
pp; 18 DwgNo 13/21

11/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014725215
WPI Acc No: 2002-545919/200258
Related WPI Acc No: 2003-843021
XRAM Acc No: C02-154711
XRPX Acc No: N02-432061

Passivation of integrated circuit devices for wire bond packaging, involves forming adhesion layer on surface of insulating layer by treating surface of insulating layer with gas

Patent Assignee: INTEL CORP (ITLC)
Inventor: **BAKKER G L; DASS M L A; SESHAN K**

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6352940	B1	20020305	US 98105590	A	19980626	200258	B

Priority Applications (No Type Date): US 98105590 A 19980626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6352940	B1		17	H01L-021/31	

Abstract (Basic): US 6352940 B1
Abstract (Basic):

NOVELTY - An integrated circuit (IC) device is passivated by forming an insulating layer (28) on a substrate (26). An adhesion layer (150) is formed into the surface of the insulating layer by treating the surface of the insulating layer with a gas. A first **passivation layer** is formed on the adhesion **layer**. The first **passivation layer** and the gas include common chemical element(s).

USE - For passivation of IC devices used in wire bond packaging.

ADVANTAGE - The inventive method improves adhesion between insulating **layer** and hard **passivation layers** of integrated circuit devices to reduce delamination that occurs during the manufacturing process of these devices, such as thermal cycling and sawing.

DESCRIPTION OF DRAWING(S) - The figures show the inventive integrated circuit devices.

Substrate (26)
Insulating layer (28)
Adhesion layer (150)
pp; 17 DwgNo 9, 10/21

13/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015681048
WPI Acc No: 2003-743237/200370
XRPX Acc No: N03-595126
Integrated circuit structure for semiconductor devices, has one terminal interconnection layers formed on another layer that includes protective structures and signal line having protective structure mounted between layers
Patent Assignee: INTEL CORP (ITLC)
Inventor: SELVIN E; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6614118	B1	20030902	US 99464058	A	19991215	200370	B

Priority Applications (No Type Date): US 99464058 A 19991215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6614118	B1		7	H01L-023/48	

Abstract (Basic): US 6614118 B1
Abstract (Basic):
NOVELTY - The circuit structure has a terminal interconnection metallization layer (M5) formed upon a substrate (230). A signal line (204) is coupled to the terminal interconnection layer and another terminal interconnection layer (M4) is formed on the former layer. The structure has a protective structure (206) that surrounds the signal line.
USE - Used for protecting integrated circuits in semiconductor circuits.
ADVANTAGE - The structure protects the integrated circuits against various types of damages e.g. mechanically protecting the circuits when the dies are packaged or subjected to temperature cycling during reliability testing.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional view of a die.
Signal line (204)
Contact structures (206, 208, 210)
Hard **passivation layer** (212)
Soft **passivation layer** (213)
Substrate (230)
Landing pads (225A, 225B, 225C, 225D)
Metallization layers (M2, M3, M4)
Contact plugs (227A, 227B, 227C, 227D, 227E)
pp; 7 DwgNo 3/4

13/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015634588
WPI Acc No: 2003-696770/200366
XRAM Acc No: C03-191408
XRPX Acc No: N03-556467
Formation of wire bond comprises forming protective structure over

metallization copper pad, and wire bonding device at second metal film
Patent Assignee: INTEL CORP (ITLC)
Inventor: **SESHAN K**; SINGH K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030132766	A1	20030717	US 200252089	A	20020116	200366	B

Priority Applications (No Type Date): US 200252089 A 20020116
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030132766	A1		12	G01R-027/08	

Abstract (Basic): US 20030132766 A1
Abstract (Basic):

NOVELTY - Wire bond is formed by, forming protective structure over metallization copper pad (114, 124), and wire bonding device at second metal film. The metallization copper pad makes contact (122) with a device. The protective structure includes a metal first film disposed above and on the metallization copper pad, and metal second film disposed above and on the metal first film.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a wire-bond configuration comprising metallization copper pad disposed over a device, protective surface disposed above on the metallization copper pad, and test probe tip or bond wire in contact with the protective structure; and

(b) a method of testing device comprising contacting test probe tip to metallization, and passing a test current that experiences ohmic resistance of 0.5-4 ohms through the test probe.

USE - For forming wire bond for metallization process flow.

ADVANTAGE - The invention minimizes copper corrosion in the copper pad or other metallization that is wire bonded.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a semiconductor structure during the formation of wire bond.

Metallization copper pad (114, 124)
Nitride first layer (118)
Passivation layer (120)
Contact (122)
pp; 12 DwgNo 1/8

13/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015460561
WPI Acc No: 2003-522703/200349
XRAM Acc No: C03-140413
XRPX Acc No: N03-414793
Semiconductor integrated circuit device e.g. microprocessor for electrical device, has **passivation layer** provided with selectively sized windows through which solder bumps extend and electrically contact metal layer
Patent Assignee: SESHAN K (SESH-I)
Inventor: **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030080406	A1	20030501	US 200122700	A	20011030	200349	B

Priority Applications (No Type Date): US 200122700 A 20011030
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030080406 A1 11 H01L-023/52

Abstract (Basic): US 20030080406 A1
Abstract (Basic):
NOVELTY - The integrated circuit (IC) device (10) includes a **passivation layer** (16) which is interposed between a metal layer (62) and several solder bumps (22). The **passivation layer** has windows (15) through which the bumps extend for electrically contacting the metal pads (66) of the metal layer. The windows are selectively sized for imparting higher or lower current capability to corresponding bumps.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) electrical device; and
(2) semiconductor integrated circuit (IC) device forming method
USE - Semiconductor integrated circuit (IC) device e.g. microprocessor used in electrical devices (claimed).
ADVANTAGE - Since the windows are selectively sized, the current carrying capability of solder bumps are accordingly varied, so that premature failure of the bumps due to electro- migration is avoided.
DESCRIPTION OF DRAWING(S) - The figure shows a cross- sectional view of the semiconductor IC device.
window (15)
passivation layer (16)
supply voltage bus (17)
solder bumps (22)
metal layer (62)
metal pads (66)
pp; 11 DwgNo 2/11

13/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014459812
WPI Acc No: 2002-280515/200232
XRAM Acc No: C02-082455
XRPX Acc No: N02-219118
Input/output for semiconductor device, e.g. microprocessor, comprises bond pad having ball limiting metallurgy containing film of nickel-vanadium-nitrogen
Patent Assignee: INTEL CORP (ITLC); SESHAN K (SESH-I)
Inventor: **SESHAN K**
Number of Countries: 096 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200203461	A2	20020110	WO 2001US18666	A	20010608	200232	B
AU 200175426	A	20020114	AU 200175426	A	20010608	200237	
US 20020079576	A1	20020627	US 2000608956	A	20000630	200245	
			US 2001999574	A	20011031		
US 6521996	B1	20030218	US 2000608956	A	20000630	200317	
EP 1334519	A2	20030813	EP 2001942135	A	20010608	200355	
			WO 2001US18666	A	20010608		
US 6610595	B2	20030826	US 2000608956	A	20000630	200357	
			US 2001999574	A	20011031		
CN 1446375	A	20031001	CN 2001811988	A	20010608	200382	

Priority Applications (No Type Date): US 2000608956 A 20000630; US 2001999574 A 20011031
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200203461 A2 E 19 H01L-023/00
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW
AU 200175426 A H01L-023/00 Based on patent WO 200203461
US 20020079576 A1 H01L-023/48 Div ex application US 2000608956
US 6521996 B1 H01L-023/48
EP 1334519 A2 E H01L-023/00 Based on patent WO 200203461
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 6610595 B2 H01L-021/44 Div ex application US 2000608956
CN 1446375 A H01L-021/60
Abstract (Basic): WO 200203461 A2
Abstract (Basic):
NOVELTY - An input/output comprises a bond pad, a ball limiting metallurgy (BLM) (222) on the bond pad, and a bump (228) on the BLM. The BLM comprises a first alloy film (226) containing nickel-vanadium-nitrogen.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the formation of an input/output on a device comprising forming an opening in a **passivation layer** on a bond pad, forming a BLM on the bond pad in the opening and on the **passivation layer**, and forming a bump on the BLM.
USE - The input/output is used for semiconductor device, e.g. microprocessor, application specific integrated circuit, field programmable gate array or system-on-a-chip to condition and distribute power, ground and signals.
ADVANTAGE - The input/output can be fabricated in a large number (preferably 600-7,000 input/outputs) across the upper surface of the device. It can support current density of 110-300 mA/bump and can withstand operating temperature of 110-120degreesC without reliability issues. It enables fabrication of semiconductor devices which require a large number of input/outputs.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the reflow of the bump on the device.
BLM (222)
First alloy film (226)
Bump (228)
pp; 19 DwgNo 2f/2

13/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013585552
WPI Acc No: 2001-069759/200108
Related WPI Acc No: 2003-370565
XRAM Acc No: C01-019292
XRPX Acc No: N01-052717
Method for exposing bond pad in integrated circuit having two **passivation layers**, involves removing portion of second

passivation layer over bond pad, curing remaining second **passivation layer** and etching exposed first **passivation layer**

Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; KARKLIN K D; ROGGEL A; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6143668	A	20001107	US 97941795	A	19970930	200108	B

Priority Applications (No Type Date): US 97941795 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6143668	A		25	H01L-021/31	

Abstract (Basic): US 6143668 A
Abstract (Basic):

NOVELTY - A bond pad (110) in an integrated circuit coated with first (120) and second (130) **passivation layers** is exposed by removing a portion of the second **passivation layer** over the bond pad, curing the remaining portions of the second **passivation layer** and etching the exposed first **passivation layer** to expose the bond pad.

USE - The method is used in fabrication of integrated circuit devices such as a probe card having a pad pitch of less than 80 micron.

ADVANTAGE - The method produces durable probe features with reliable contacts to bond pads having a low pad pitch.

DESCRIPTION OF DRAWING(S) - The drawing shows a stage for removal of the first **passivation layer**.

Aluminum bond pad (110)
Hard **passivation layer** (120)
Photodefinable polyimide **passivation layer** (130)
Residual layer following the polyimide curing step (140)
pp; 25 DwgNo 14/24

13/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013144897
WPI Acc No: 2000-316769/200027
XRAM Acc No: C00-095704
XRPX Acc No: N00-237763
Passivating integrated circuit comprises depositing silicon nitride over a top surface portion of the circuit, and treating the exposed surface to form silicon oxynitride

Patent Assignee: INTEL CORP (ITLC)
Inventor: **DASS M L A**; GAETA I; **SESHAN K**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6046101	A	20000404	US 971970	A	19971231	200027	B

Priority Applications (No Type Date): US 971970 A 19971231
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6046101	A		13	H01L-021/318	

Abstract (Basic): US 6046101 A

Abstract (Basic):
NOVELTY - Integrated circuit is passivated by depositing a silicon nitride layer over the top surface of a portion of an integrated circuit, treating an exposed surface of the first **passivation layer** to form a silicon oxynitride layer and depositing a second passivation **layer** over the first **passivation layer**.
USE - For passivating integrated circuit.
ADVANTAGE - Delamination is minimized by eliminating passivation material from the scribe street area prior to separating devices and the combined passivation technology has robust **passivation** resistance to thin **film** delamination.
pp; 13 DwgNo 0/21

13/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012599475
WPI Acc No: 1999-405581/199934
XRAM Acc No: C99-119865
XRPX Acc No: N99-302307
Integrated circuit with an improved guard ring structure to prevent damage
Patent Assignee: INTEL CORP (ITLC)
Inventor: MIELKE N R; **SESHAN K**
Number of Countries: 084 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9934440	A1	19990708	WO 98US25467	A	19981201	199934	B
AU 9916162	A	19990719	AU 9916162	A	19981201	199951	
US 6137155	A	20001024	US 971397	A	19971231	200055	
TW 436924	A	20010528	TW 98121632	A	19981224	200172	
US 6376899	B1	20020423	US 971397	A	19971231	200232	
			US 2000651367	A	20000829		

Priority Applications (No Type Date): US 971397 A 19971231; US 2000651367 A 20000829
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9934440	A1	E	24	H01L-023/485	
Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9916162	A			H01L-023/485	Based on patent WO 9934440
US 6137155	A			H01L-023/58	
TW 436924	A			H01L-021/31	
US 6376899	B1			H01L-023/544	Cont of application US 971397 Cont of patent US 6137155

Abstract (Basic): WO 9934440 A1
Abstract (Basic):
NOVELTY - The integrated circuit has a planar **passivating layer** formed on the terminal dielectric layer. This avoids the possibility of damage to the nitride layer caused by reentrant angles had the terminal metal layer with a guard ring protruded outside the terminal dielectric layer as is current practice.

DETAILED DESCRIPTION - Integrated circuit comprises: (a) substrate with at least one dielectric layer and metal layer formed on it, with the dielectric layer including a terminal dielectric **layer**; (b) planar **passivating layer** formed on the terminal dielectric layer.

USE - Integrated circuits.

ADVANTAGE - The planar **passivating layer** eliminates the problems of instability of guard rings formed in terminal metal layers.

DESCRIPTION OF DRAWING(S) - The drawings show a top view of an integrated circuit.

Die active area (501)
Via (504)
Planar **passivating** nitride **layer** (506)
Terminal dielectric layer (508, ILD4)
Guard wall (526)
Side of die (575)
Vias (V1-4)
Metal layers (M1-4)
Interlevel dielectric (ILD3)
pp; 24 DwgNo 5/8

13/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012449126
WPI Acc No: 1999-255234/199921
XRAM Acc No: C99-074783
XRPX Acc No: N99-190009
Integrated circuit structure on a silicon wafer substrate
Patent Assignee: INTEL CORP (ITLC)
Inventor: **SESHAN K**
Number of Countries: 083 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9917365	A1	19990408	WO 98US13561	A	19980629	199921	B
AU 9882753	A	19990423	AU 9882753	A	19980629	199935	
US 6043551	A	20000328	US 97940535	A	19970930	200023	
GB 2345384	A	20000705	WO 98US13561	A	19980629	200035	
			GB 20007667	A	20000329		
TW 429508	A	20010411	TW 98111410	A	19980714	200157	
GB 2345384	B	20021106	WO 98US13561	A	19980629	200281	
			GB 20007667	A	20000329		

Priority Applications (No Type Date): US 97940535 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9917365	A1	E	35	H01L-023/52	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9882753	A		Based on patent WO 9917365
US 6043551	A	H01L-027/095	
GB 2345384	A	H01L-023/58	Based on patent WO 9917365
TW 429508	A	H01L-021/76	
GB 2345384	B	H01L-023/58	Based on patent WO 9917365

Abstract (Basic): WO 9917365 A1

Abstract (Basic):

NOVELTY - The integrated circuit has electrically isolated metal structure formed by patterning and etching the terminal metal layer used to form a die active area. The locking structures adhere to the overlying passivation and prevent its delamination.

DETAILED DESCRIPTION - Integrated circuit includes a silicon substrate; dielectric layer and terminal metal layer (TML), with the dielectric and TML layers forming a die active area. The TML has a number of locking structures electrically isolated from one another and outside the die active area. A **passivation layer** adheres to the locking structures.

INDEPENDENT CLAIMS are included for the following:

(i) a method of forming a sealed computer chip by:

(a) forming a number of electrical circuits on a silicon wafer by forming device and interconnect layers including TML;

(b) forming a guard ring from the TML enclosing the die active area;

(c) forming spaced apart locking structures enclosed by the guard ring but outside the die active area;

(d) depositing a **passivation layer** over the locking structures and guard ring;

(ii) the integrated circuit as above in which each metal locking structure is located near the IC edge connected to a voltage supply;

(iii) a method of fabricating a sealed computer chip by:

(a) forming a number of electrical circuits on a silicon wafer by forming device and interconnect layers including TML;

(b) forming a guard ring from the TML enclosing the die active area;

(c) forming spaced apart locking structures from the TML, each locking structure coupled to a voltage supply Vss of integrated circuit;

(d) depositing a **passivation layer** over the locking structures and guard ring;

(iv) a device as above including a number of dielectric and metal layers forming a die active area, the dielectric layers and metal layers including terminal dielectric (TDL) and metal (TML) layers.

USE - Fabrication of integrated circuits.

ADVANTAGE - The structure reduces the possibility of sawing cuts through the guard wall and prevents interlayer delamination.

DESCRIPTION OF DRAWING(S) - The drawing shows an integrated circuit of the invention.

Die active area (501)
Terminal metal layer (502)
Terminal dielectric layer (503)
Contiguous guard ring (504)
Locking structure (506)
Corners (550)
Edges (575)
Pattern recognition structures (580)
Voltage supply (Vss)
pp; 35 DwgNo 5/12

13/3,AB/9 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012449116

WPI Acc No: 1999-255224/199921
XRAM Acc No: C99-074776
XRPX Acc No: N99-189999
Integrated circuit structure on a silicon wafer substrate
Patent Assignee: INTEL CORP (ITLC)
Inventor: MIELKE N R; **SESHAN K**
Number of Countries: 084 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9917348	A1	19990408	WO 98US14023	A	19980706	199921	B
AU 9882916	A	19990423	AU 9882916	A	19980706	199935	
US 5977639	A	19991102	US 97940304	A	19970930	199953	
GB 2345580	A	20000712	WO 98US14023	A	19980706	200035	
			GB 20007669	A	20000329		
TW 409370	A	20001021	TW 98111409	A	19980714	200121	
GB 2345580	B	20020703	WO 98US14023	A	19980706	200251	
			GB 20007669	A	20000329		

Priority Applications (No Type Date): US 97940304 A 19970930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9917348	A1	E	32	H01L-021/283	

Designated States (National): AL AM AT AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9882916	A		Based on patent WO 9917348
US 5977639	A	H01L-023/48	
GB 2345580	A	H01L-023/58	Based on patent WO 9917348
TW 409370	A	H01L-021/8252	
GB 2345580	B	H01L-023/58	Based on patent WO 9917348

Abstract (Basic): WO 9917348 A1
Abstract (Basic):
NOVELTY - The integrated circuit has electrically isolated metal staples formed by patterning and etching the terminal metal layer used to form a die active area. The locking structures adhere to the overlying passivation and prevent its delamination by providing increased surface area for adherence.
DETAILED DESCRIPTION - Integrated circuit comprises in order: silicon substrate; a number of dielectric and metal layers forming a die active area, the metal layers having a guard wall surrounding the die active area and the metal layers having a segmented guard wall surrounding the first guard wall and stapling the metal **layers**. A **passivation layer** adheres to the first and the segmented guard wall.
USE - Fabrication of integrated circuits.
ADVANTAGE - The structure reduces the possibility of sawing cuts through the guard wall and prevents interlayer delamination.
DESCRIPTION OF DRAWING(S) - The drawing shows an integrated circuit of the invention.
Die active area (501)
Terminal metal layer (502)
Guard ring (504)
Locking structures (506)
Guard wall (508)
Lateral surfaces (511)
Top surface (531)

Metal layers with interposed dielectric layers (M1 - M5)
pp; 32 DwgNo 6/12

EIC 113928

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 2/9/04 Serial # 10/013,103 Priority Application Date 4/26/98

Your Name W. Lewis Examiner # _____

AU 2822 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

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Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___ _____
Teaching Refs ___ _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 17-21

Please focus on claim 21 + 24 +
ignore "by treating" aspects.

Problem: See Paper 2 lines 6-9 of
" " 3 " 1-6

Solution: " " 4 " 1-6

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Searcher: Speckhard	Structure (#) ___	STN ✓
Searcher Phone: ___	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation ___	Questel/Orbit ___
Date Searcher Picked Up: 2/13/04	Fulltext ___	Lexis-Nexis ___
Date Completed: 2/13/04	Patent Family ✓	WWW/Internet ___
Searcher Prep/Rev Time: 190	Other et at., au	Other ___
Online Time: 90		